FinFET based Analog Circuits: A Paradigm Change in Circuit Analysis

Summary: Complementary metal oxide semiconductor (CMOS) integrated circuits (ICs) have seen overwhelming growth in electronic industry with gadgets for entertainment, communication, computing, signal processing and other applications. Low power consumption, reduced area, increased speed and lower production cost per chip etc., are some advantages of CMOS technology that have opened the door for integration of millions of transistors on a single chip. It is also believed that, with technology scaling, the trend of rapid improvements in performance of CMOS ICs will continue in near future. Advancement in CMOS technology in modern times has further ensured not only higher packing density but also improved performance in digital, analog and mixed signal circuit design. This tutorial will deal with the application of FinFET which has matured at 22 nm technology node for mixed signal applications.

Topics to be covered

1. Introduction to Multigate MOSFETs
2. Introduction to FinFET, High-k gate and spacer dielectric, Advantages/Issues
3. Analog performance study
4. Design and Analysis at scaled gate lengths, Variability Issues
5. Spatial variation effect of (Tox and Xj) on analog FOM of OTA
6. Low temperature operation and scaling issues
7. Analytical model development for dual-k underlap FinFET
8. Introduction of S/D lateral profile on analytical model of DGMOSFET

Speaker Profile

S. Dasgupta, is presently working as an Associate Professor, in the Department of Electronics and Communication Engineering at Indian Institute of Technology, Roorkee. He received his PhD degree in Electronics Engineering from IIT-Banaras Hindu University, Varanasi in 2000. During his PhD work, he carried out research in the area of effects of ionizing radiation on MOSFET. Subsequently, he was member of faculty of Department of Electronics Engg.,at Indian School of Mines, Dhanbad (IITDhanbad). In 2006, he joined as an Assistant Professor in the Department of Electronics and Communication Engineering at Indian Institute of Technology, Roorkee. He is currently also the Chairman, Faculty Search Committee of the Department. He has authored/co-authored more than 200 research papers in peer reviewed international journals and conferences. He is a member of IEEE, EDS, ISTE and associate member of Institute of Nanotechnology, UK. He has been a technical committee member International Conference on Micro-to-Nano, 2006; he is also been nominated as Marquis’s Who’s Who in Science in Engineering, USA awarded by Marquis, 2006, 2007 and 2008 and has been acting as an expert member of The Global Open University, The Netherlands. He was awarded with Erasmus Mundus Fellowship of European Union in the year 2010 to work in the area of RDF at Politecnico Di Torino, Italy. He is the recipient of prestigious IUSSTF to work in the area of SRAM testing at University of Wisconsin at Madison, USA in the year 2011-12. He was also awarded with DAAD Fellowship to work on Analog Design using Reconfigurable Logic at TU, Dresden, Germany in the year 2013. His areas of interest are
Nanoelectronics, Nanoscale MOSFET modeling and simulation, Design and Development of low power novel devices, FinFET based Memory Design, Emerging Devices in Analog Design and Design and development of reconfigurable logic. He has guided 12 Ph.D scholars. Currently he is supervising around 6 candidates leading to their Ph.D degree. He has been nominated for INAE, Young Engineer Award. Dr. Dasgupta acted as a reviewer for IEEE Transactions on Electron Devices, IEEE Transactions on VLSI Systems, IEEE Electron Device Letters, IEEE Transactions on Nanotechnology, Superlattice and Microstructures, International Journal of Electronics, Semiconductor Science and Technology, Nanotechnology, Microelectronic Engineering, Microelectronic Reliability amongst other. He has also been member of technical committees of various international conferences. He has presented tutorial in VDAT-2014 and VLSI Design Conference, Bangalore 2015 amongst many others.